CLAIMS

1. An integrated clock system, comprising:

a reference voltage;

a transconductor element coupled to receive a reference voltage from the reference voltage source;

a capacitive element coupled to receive a proportional voltage output from the transconductor element, the capacitive element comprising a plurality of capacitors, each of which is selectable; and

a comparator coupled to receive the reference voltage from the voltage reference source and also coupled to receive a voltage that is across the terminals of the capacitor circuitry wherein the comparator generates a reset signal to cause a capacitor circuit to be discharged or reset whenever the voltage across the capacitor circuit matches the reference voltage.

2. The system of claim 1 wherein the comparator circuit includes a resistive element on an input side that is coupled to receive the reference voltage.

3. The system of claim 1 wherein the capacitor circuitry is coupled in parallel to the transconductor element.

4. The system of claim 1 wherein the capacitor circuit comprises more than ten capacitors.

5. The system of claim 1 wherein the capacitor circuit comprises at least thirty-two capacitors.

6. The system of claim 1 wherein each capacitor is coupled in series with a switch, which switch is controlled by an external controller to switch the corresponding capacitor in or out of the circuit.

7. The system of claim 1 wherein the capacitor circuit includes exactly thirty-two capacitors.

8. A system for calibrating the RC time constant of an integrated clock, comprising:

a register for storing a reset number;

a counter coupled to receive a reset number from the register and further coupled to receive clock cycles from an RC oscillator;

a master counter for receiving a reset signal from the counter, which reset signal is generated by the counter whenever the number of clock cycles that is received from the RC oscillator matches the reset number received from the register;

the master counter being further coupled to receive clock signals from a master clock, which master counter generates a count value, which count value reflects the number of clock cycles received from the master clock since the last reset signal was received; and

calibration circuitry coupled to receive the count value from the master counter wherein the calibration logic generates control signals to the RC oscillator to increase or decrease the RC time constant according to the value received in the count signal from the master counter.

9. A system of claim 8 wherein the register stores a reset number that is equal to 1,000.

10. The system of claim 8 wherein the calibration circuitry generates a signal to increase the RC time constant if the value of the count number received from the master counter is greater than 1,000.

11. The system of claim 8 wherein the calibration circuitry generates a signal to decrease the RC time constant if the value of the count number received from the master counter is less than 1,000.

12. The system of claim 8 wherein the calibration circuit includes logic to increase the RC time constant of the RC oscillator by generating signals to increase the capacitance therein.

13. The system of claim 8 wherein the calibration circuit includes logic to decrease the RC time constant of the RC oscillator by generating signals to decrease the capacitance therein.

14. The system of claim 8 wherein the RC time constant is adjusted by switching capacitors of a capacitor array in or out of connectivity within the RC oscillator according to whether an RC time constant requires increasing or decreasing to cause the oscillator to produce a desired frequency of operation.

15. A method for adjusting an RC time constant in an oscillator, comprising:

setting a capacitor array to an initial first value of capacitance;

receiving a count value;

determining whether the RC time constant is low;

if the RC time constant is low, incrementing the capacitance value to a new value;

if the RC time constant is not low, determining the whether the RC time constant is high; and

if the RC time constant is high, decrementing the capacitance to a new value.

16. The method of claim 12 further comprising the step of determining if the change included a minimal step size.

17. The method of claim 12 wherein the new value is approximately one-half of the possible amount of capacitance that may be changed from a present value to a maximum value.

18. The method of claim 12 wherein the new value is a value that is approximately one-half of the possible amount of capacitance that may be changed from the present value to a minimum value.

19. The method of claim 15 wherein the RC time constant value is determined to be low if a count value is higher than a specified number.

20. The method of claim 15 wherein the RC time constant value is determined to be high if a count value is lower than a specified number.

21. The method of claim 15 wherein the initial value is one that is approximately half of the total amount of capacitance that may be set within the capacitor array.